THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RIICHIRO SHIROTA and MASAKI MOMODOMI

Appeal No. 1997-3442
Application No. 08/210,288[1]

HEARD: January 13, 2000

Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 9. Claims 14 through 16 have been allowed and claims 10 through 13 have been indicated by the examiner as being directed to allowable subject matter.

[1] Application for patent filed March 18, 1994.

The invention pertains to a non-volatile semiconductor memory device, best described by reference to Figure 7A and to independent claim 1 reproduced as follows:

1. A nonvolatile semiconductor memory device comprising:

a plurality of NAND memory cells each having first and second terminals and constituted by connecting a plurality of memory cells each having a control gate in series with each other, said NAND memory cells including adjacent first and second NAND memory cells;

bit lines commonly used for NAND memory sets each constituted by at least said first and second NAND memory cells of said NAND memory cells, said bit lines being coupled to the first terminals of said NAND memory cells;

source lines commonly used for the NAND memory set each constituted by at least said first and second NAND memory cells of said NAND memory cells, said source lines being coupled to the second terminals of said NAND memory cells;

first selection transistors arranged between the first terminal of the first NAND memory cell and said bit line;

second selection transistors arranged between the first terminal of said second NAND memory cell and said bit line;

third selection transistors arranged between the second terminal of the first NAND memory cell and said source line;

fourth selection transistors arranged between the second terminal of said second NAND memory cell and said source line;

a first control gate line coupled to at least control gates of said first selection transistors;

a second control gate line coupled to at least control gates of said second selection transistors;

a third control gate line coupled to at least control gates of said third selection transistors;

a fourth control gate line coupled to at least control gates of said fourth selection transistors.

The examiner relies on the following references:

Choi et al. (Choi) 4,962,481 Oct. 9, 1990

E. Adler, "Densely Arrayed EEPROM Having Low-Voltage Tunnel Write", IBM TDB, Vol. 27, No. 6 pp. 3302-3307, Nov. 1984

Japanese Patent Application
Kanazawa[2] 02-74069 Mar. 14, 1990

Claims 1, 3, 4 and 6 through 8 stand rejected under 35 U.S.C. 102(b) as anticipated by Adler. Claims 2, 5 and 9 stand rejected under 35 U.S.C. 103 as unpatentable over Adler in view of either one of Choi or Kanazawa.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

At the outset, we note our displeasure with the way the examiner sets forth the rejection in the answer. M.P.E.P. 1208

[2] Our understanding of this reference is based on an English translation thereof prepared by the United States Patent and Trademark Office. A copy of this translation is attached hereto.

permits an examiner to refer back to a *single* prior office action in order to incorporate the grounds of rejection into the answer. The examiner, however, refers back to the final rejection which, in turn, refers back to the "Office Action of Paper No. 7."

We reverse.

A rejection under 35 U.S.C. 102, based on anticipation, is proper only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. V. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984).

With respect to independent claim 1, the examiner applies Figure 1 of Adler, identifying word block WB1 and word block WB0 as the claimed NAND memory cells; B0 as the claimed bit lines; and Q GND as the claimed source lines. Further, on a marked-up copy of Adler's Figure 1, submitted with the answer, the examiner identifies four transistors (transistors 1 and 3 being within word block WB1 and transistors 2 and 4 being

within word block WB0) as corresponding to the claimed first, second, third and fourth selection transistors.

Appellants argue that the instant invention provides for selection transistors which independently connect/disconnect the first and second NAND memory cells to the bit/source lines by gate lines SG1-SG4. Appellants provide a further argument regarding a certain order of gate lines of the NAND memory cells in Adler [principal brief, page 7]. Since independent claim 1 is not concerned with any such "order" and the claim recites nothing about the transistors independently connecting or disconnecting the first and second NAND memory cells, appellants' arguments in these regards are not persuasive.

However, independent claim 1 is very clear on the specific and various connections of the source and bit lines, first and second terminals of the NAND memory cells and the selection transistors, as well as the control gate lines. The examiner has not clearly indicated how each of these recited connections is met by Adler. For example, it is clear from the claim language that the various recited selection transistors are connected to different terminals of the NAND memory cells and bit and source lines. As appellants point out in the reply

brief, the examiner has indicated, on the marked-up copy of Figure 1 of Adler, that the word blocks, or NAND memory cells themselves, include the first to fourth selection transistors. This is contrary to the claimed invention which clearly indicates that these selection transistors are elements separate from the NAND memory cells. Therefore, since the transistors identified by the examiner in Adler as the claimed selection transistors are not arranged in the same manner as required by independent claim 1, i.e., between terminals of the NAND memory cells and bit or source lines, Adler cannot be said to anticipate the instant claimed invention.

Accordingly, the examiner's rejection of claims 1, 3, 4 and 6 through 8 under 35 U.S.C. 102(b) will not be sustained.

With regard to the rejections of claims 2, 5 and 9 under 35 U.S.C. 103, we also will not sustain these rejections because Choi and/or Kanazawa do not provide for nor suggest the deficiencies noted supra with regard to Adler. Therefore, we do not reach dependent claims 2, 5 and 9.

The examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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